AND8402

Thermal Considerations for the NCS5650

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APPLICATION NOTE

Overview

The purpose of this report is to present and discuss essential thermal considerations regarding the use of the NCS5650 in real−world applications. The NCS5650 (a 2 A PLC Line Driver with Programmable 4th−Order Filtering, Output Current Warning/Limit plus Thermal Diagnostic Flags and Enable/Shutdown Control) comes in a 20−lead QFN (4x4 mm). To enable optimal thermal performance, this package has an exposed heatsink designed to be soldered directly to a metal pad on the application board. It will be shown that *board* thermal properties dominate the typical system in which the NCS5650 might be used. Therefore, external design choices will, in most cases, make the difference between what would otherwise be reasonable, plausible or impossible applications, at least when viewed from a strictly thermal perspective.

The junction−to−back−of−flag thermal resistance of the NCS5650 ranges from 6°C/W (if measured to the hottest point on the board−side of the exposed mounting pad), to 8°C/W (if measured to the perimeter of the exposed pad (Note 1)). On the other hand, because of the small footprint of the package, board−to−ambient thermal resistance (which is controlled by board size, materials, layout, and thermal boundary conditions), can easily range from about 15°C/W up to in excess of 120°C/W. θ_{JA} (junction to ambient, the sum of the junction−to−board contribution and the board−to−ambient contribution) thus may vary nearly an order of magnitude, from the most optimistic, thermally aggressive value of about 20°C/W, up to 130°C/W. Conceivably, even lower values could be achieved by the use of forced−convection cooling applied to external heatsinks on the back side of the application board, yet on the other hand, values much worse than 130°C/W could be realized if insufficient board area is provided for the device. The latter possibility may arise indirectly and inadvertently, for instance, if other heat sources exist in close proximity to the NCS5650, effectively “stealing” some of the convection area from the NCS5650.

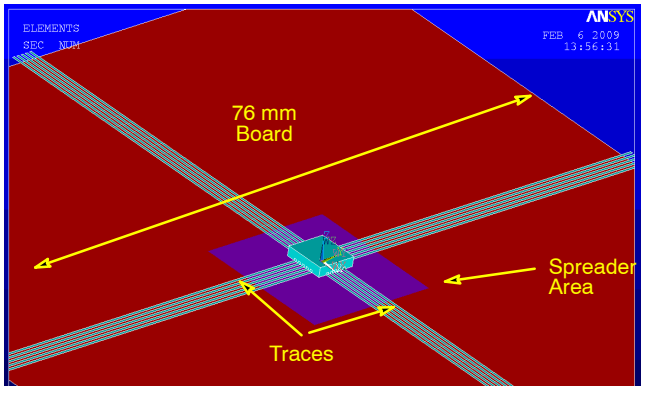

Figure 1. Spreader Area Centered Around QFN shown through transparent board

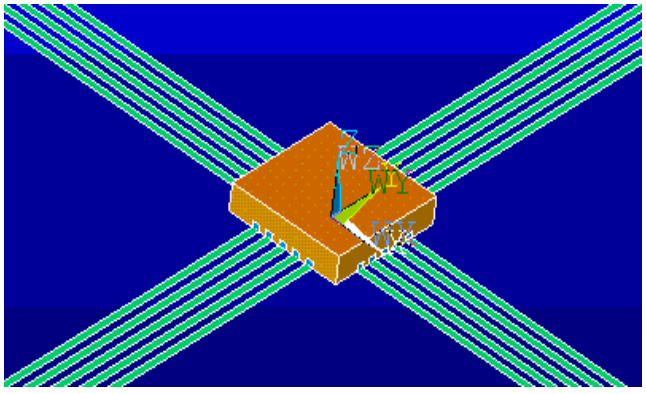

Figure 2. 4x4 QFN Showing Traces to Each Lead each trace 35 um thick (1 oz) by 0.25 mm wide

1. The standard QFN manufacturing process incorporates a thermally enhanced epoxy for die attach. If solder is an option, these junction−to−back−of−flag thermal resistances drop to the 3−5°C/W range.

Without resorting to *extraordinary* thermal effort (for example, external heatsinks with forced air movement on the back side of the board), this report will describe how thermal performance of the NCS5650 varies on a square 76 mm (3”) application board, where three primary variables are considered:

1. The nature of thermal vias which may be provided under the exposed pad of the device;
2. The thickness of a thermal spreading plane, located either on the back side of the PCB, or possibly buried within the application board, if a multilayer PCB;
3. The area covered by this spreading plane.

As already mentioned, what is held constant in the analysis is the overall board size, and the thermal boundary conditions, by which is meant simply the nature of the convection from the surfaces of the board. We assume, for this analysis, that thermal ambient is represented by “still” air, the board is horizontal (with respect to gravity, which affects the motion of the “still” air in the real world), and there exists a uniform heat transfer coefficient from the exposed board surfaces. There are no additional heat sources on the board, the NCS5650 is centrally located, and the spreader is centered around the package (albeit on the back side of the board – Figure 1). Board thicknesses of 1.57 and 0.79 mm were analyzed for gross effect. Finally, it is assumed that each of the 20 leads has a dedicated copper trace 35 um thick (Figure 2).

Definitions

θ_{JA} = [(temperature at junction) − (ambient)]/(total power dissipation)

Ψ_{JB} = [(temperature at junction) − (temperature at board)]/(total power dissipation)

Ψ_{BA} = [(temperature at board) − (ambient)]/(total power dissipation)

Terminology and Package Basics

In the definitions above, note that two different terms are used, theta (Greek letter θ), and psi (Greek letter Ψ). These are in keeping with current JEDEC terminology (see, for instance, JESD 51−12, published in 2005), in which θ is now reserved to refer to true thermal resistances, whereas Ψ is used whenever a resistance−like parameter appears having units of thermal resistance, but not being a true path resistance. In this analysis, since the entire thermal system is included, 100% of the power dissipated at the device junction flows all the way to ambient, hence θ_{JA} is the proper term. If we refer to the junction−to−board resistance, however, we’re really referring to Ψ_{JB}, not θ_{JB} (similarly for the board to ambient resistance,Ψ_{BA}), because if we divide the temperature difference between junction and board (or between board and ambient) by the *total* package power dissipation, we have overlooked the fact that a fraction of total device power escapes through the upper surface (and sides) of the device. As this fraction of the power does not actually flow through the board, one underestimates the corresponding actual path resistances. It is not particularly important for *this* analysis, since total system performance is being monitored (θ_{JA}); yet if we were focusing entirely on the board−to−ambient system performance, the distinction would become significant when the heat path downwards through the board is relatively poor (for example, when there is no heat spreader, or there are no thermal vias).

Thermal Vias

In the past, when package sizes were considerably larger than they are today, large power dissipating devices, besides having larger cases in general, could often be readily mounted on large external heatsinks. Even when surface−mounted on a PCB, one could, as a first−order approximation, neglect the influence of the relatively thin PCB material under a device, rightly assuming the heat was spread out over a large area before it had to penetrate the board. With much smaller packages, however (the 4x4 QFN being the specific example of interest) the exposed flag size may not be many times the thickness of the PCB. (Consider that the exposed pad of the 4x4 QFN is only 2.7 mm wide, less than twice the size of a standard 1.5 mm PCB thickness.) So not only is the area of the package smaller (implying that for the same thermal dissipation capability it must be thermally connected to a much larger area, indeed, an area just as large as used to be available to the larger packages), but because the package is small in comparison to the PCB thickness, heat will spread as it penetrates – yet PCB materials are notoriously poor thermal conductors. For this reason, thermal vias are a very important consideration in a thermally sensitive design. In the past, thermal vias might make only a marginal improvement in overall system thermal performance; by contrast, in an application using a small surface−mount device such as the NCS5650, properly designed thermal vias can cut the thermal resistance of the system in half, under optimal circumstances.

Thermal vias, unfortunately, are *not* all created equal. Outside diameter, inside diameter, wall material, whether the vias are filled or hollow (and what they’re filled with, if filled), board thickness, and of course, the number of vias, all have significant influence on the end results. Throw in the other primary variables already known to matter (spreader area and thickness, board size, airflow options, and so forth), and this is far too many variables to include in a simple thermal analysis, or to exercise in a numerical simulation (even when the simulation is very fast). To simplify the influence of thermal vias on a proposed NCS5650 application, therefore, a somewhat different approach is recommended. Figure 3 illustrates the essential variables used.

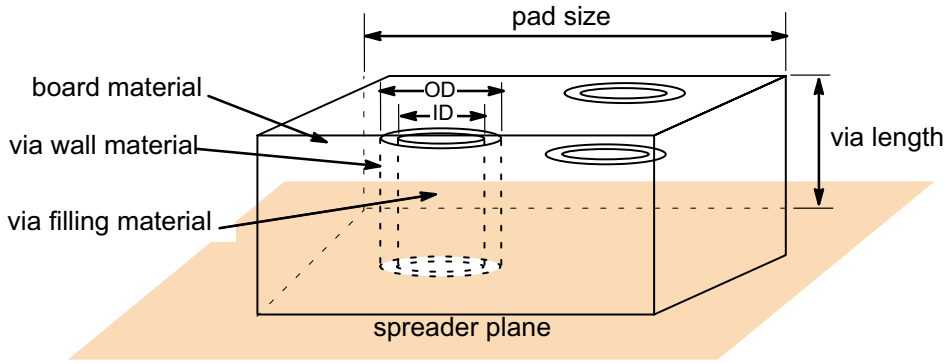

Figure 3. Primary Variables in Simplifying Thermal via Influence

The thermal analysis assumes that thermal vias are all located under the exposed pad of the NCS5650, and that the only significant heat transfer due to the *vias* is axial (i.e., purely vertically from the pad to the spreader). Instead of modeling individual vias, however, and having to track all the aforementioned independent variables, the vertical (perpendicular−to−plane) conductivity of the board material is modified to reflect the presence of the vias. As the diameter, wall thickness, and number of vias increase, the equivalent vertical conductivity of the via−composite board material increases. Note that this composite board material fills up the entire board thickness to the full length and width of the exposed flag/pad of the device.

Also note that the horizontal (in−plane) conductivity of the composite board material is left unchanged at the standard pure−board value. Because board conductivity is typically so poor compared to copper (the traditional material comprising the via walls), there will be no effective spreading of heat *between* vias as it passes through the board. Rather, some amount of spreading is presumed to occur within the device itself (enhanced somewhat by the exposed pad on the board to which the device is soldered) – this spreading is explicitly accounted for in the model. Further spreading is assumed to occur once the heat arrives at the spreader plane, which is also accounted for in the model. With invariant in−plane conductivity, in the limiting case of no vias, the model obviously will degenerate correctly to "pure" PCB material with its standard conductivity. As vias are added, the heat flow horizontally within the composite region will not be exactly correct, but with vias, so much more heat travels directly down to the spreader that the spreader's horizontal conduction totally overtakes the influence of the board's (or composite material's) horizontal conductivity. Comparing the results between the two different board thicknesses, one observes that a thinner board will have a small thermal advantage when spreader area gets large and the vias are plentiful, whereas the thicker board will have an advantage for small spreaders and minimal vias. The explanation is that even though the board material is a poor conductor, heat spreads in the plane of the board slightly more efficiently with a thicker board, thus accessing a small spreader more effectively. It is unlikely, however, that small spreaders will yield necessary system thermal performance in most cases, so the point is somewhat moot.

In any event, many different detailed via models may be collapsed into a single master model by computing an equivalent vertical conductivity of the via−composite material, such that the vertical thermal conductivity of the resulting solid block of material equals what would be the parallel vertical thermal conductance of all the vias, in parallel with whatever they're filled with, in parallel with the board material not replaced by vias. It terms of thermal conduction (as parallel paths simply add), we may say:

$$\frac{k_{eq}s^2}{t_{b-model}} = \frac{k_f\left(n\,\pi r_i{}^2\right)}{t_{via}} + \frac{k_w\left(n\,\pi r_o{}^2 - n\,\pi r_i{}^2\right)}{t_{via}} + \frac{k_b\left(s^2 - n\,\pi r_o{}^2\right)}{t_{via}} \quad \text{(eq. 1)}$$

Equation 1 may be solved for the equivalent conductivity, and terms grouped on the right as factors associated with each of the three contributing material conductivities, thus:

$$k_{eq} = \left[k_f n\,\pi\frac{r_i{}^2}{s^2} + k_w n\,\pi\left(\frac{r_o{}^2}{s^2} - \frac{r_i{}^2}{s^2}\right) + k_b\left(1 - n\,\pi\frac{r_o{}^2}{s^2}\right)\right] \times \frac{t_{b-model}}{t_{via}} \quad \text{(eq. 2)}$$

In the preceding equations, the following meanings are assigned:

k_{eq}	equivalent conductivity of composite via block material (should be as large as possible for maximum heat transfer from top to bottom of board)
k_f	thru−plane thermal conductivity of via filler material (typical values discussed in text)
k_w	thru−plane thermal conductivity of walls (copper is taken as 380 W/m/°C)
k_b	thru−plane thermal conductivity of board material (FR4 taken as 0.343 W/m/°C)
s	flag/mounting pad size of 4x4 QFN (2.75 mm in this analysis)

r_o outer radius of vias, presumably the drill size (half the outer diameter, obviously)

r_i inner radius of vias (half the inner diameter), presumably r_o less the plating thickness

n number of vias (nine 0.3 mm diameter vias may be placed in a 3x3 grid under a 2.75 mm pad)

t_{via} via length; distance to actual spreader plane (may be total board thickness)

$t_{b-model}$ via length *as modeled*.

In this report, two discrete values for board thickness were actually modeled (0.79 mm and 1.57 mm), both having the spreader plane on the back surface of the board. Those results show, as mentioned previously, that *true* distance to the spreader plane is not entirely irrelevant, regardless of the equivalent vertical conductivity of the via region. Thus, should the real−world design incorporate an *internal* heat spreading plane, rather than the back surface of the board, the true distance to the spreader plane should be used for t_{via}, and whichever model is closer to the actual board thickness should be chosen for $t_{b-model}$. For board thickness values between the two modeled values, this will ambiguously result in two k_{eq} values differing by a factor of two, which might seem to be an extraordinarily large factor. It will be seen, however, that in most cases of interest, by the time spreader size and k_{eq} are large enough to ensure necessary system thermal performance, the resulting influence on θ_{JA} is surprisingly little.

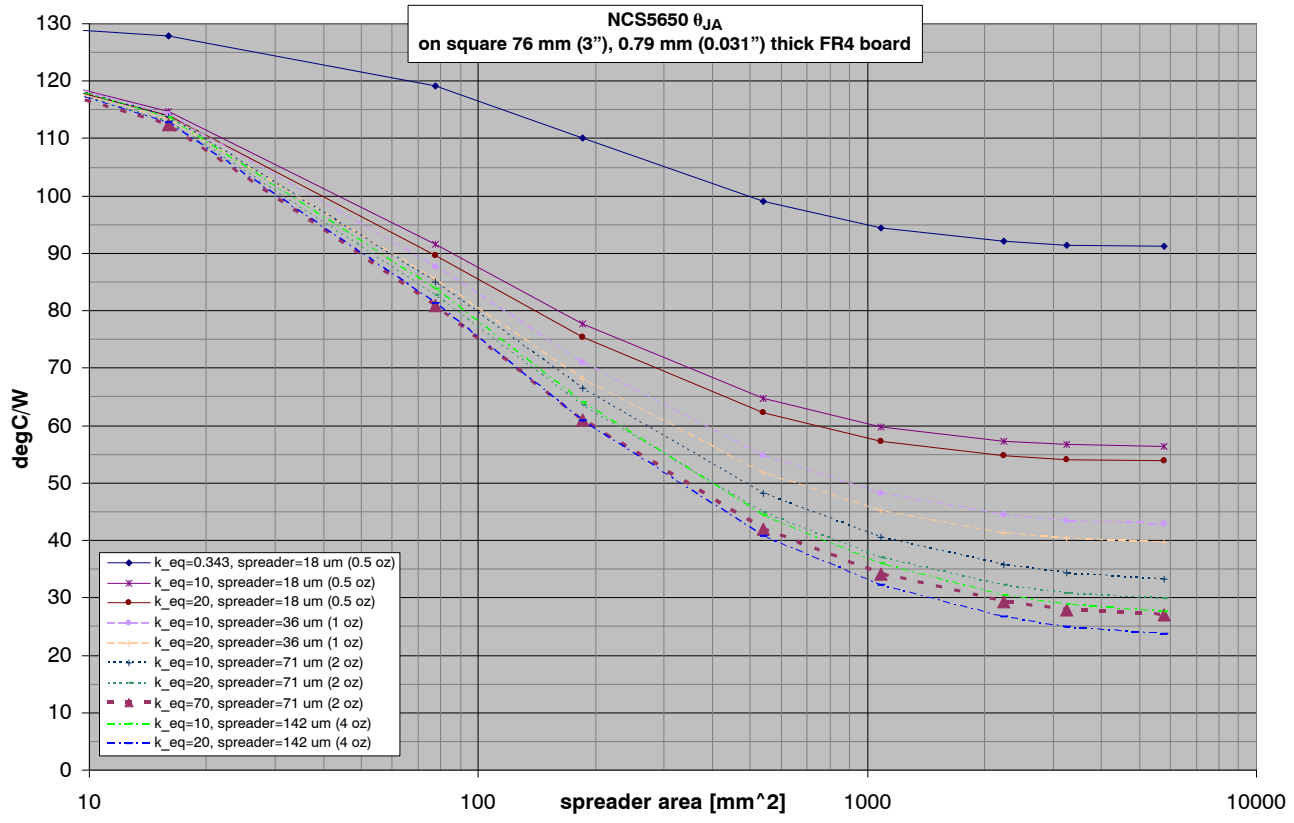

Figure 4. θ_{JA} of NCS5650 on Square 76 mm (3”), 0.79 mm (0.031”) Thick FR4 board

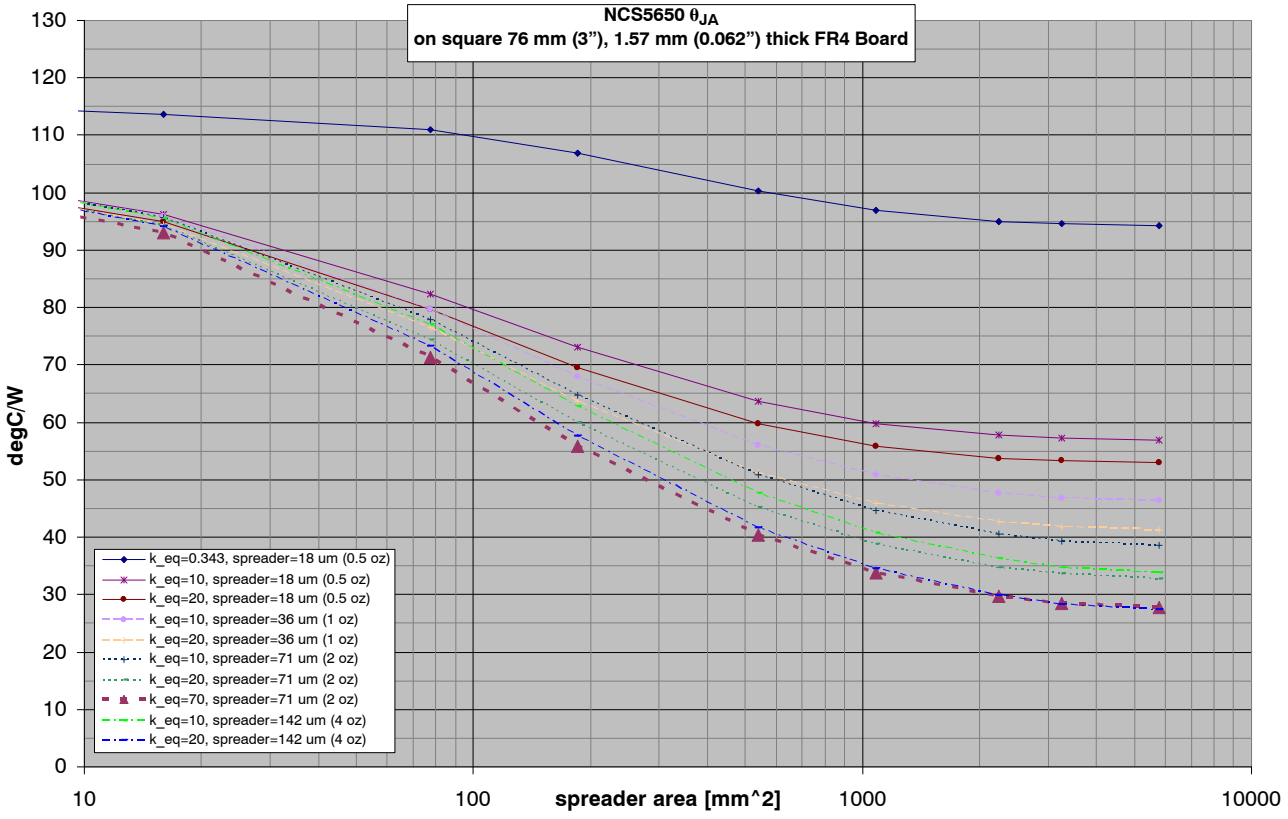

Figure 5. θ_{JA} of NCS5650 on Square 76 mm (3”), 1.57 mm (0.062”) Thick FR4 board

In Figures 4 and 5, representative θ_{JA} curves for the NCS5650 are shown. Clearly, as mentioned in the introduction, the range of end results is quite extreme, mediated significantly by available spreader area and via design (reflected primarily through the value of k_{eq}). In using these charts, keep in mind that the horizontal axis is spreader *area*, not the linear edge−dimension of the spreader. To put things in perspective, the 4x4 mm QFN footprint is 16 mm^2, 1 in^2 = 645 mm^2, and the square 76 mm board has a total area of 5800 mm^2. In the two charts, note that the “k_eq = 70, 2.0 oz” lines are emphasized. They show very nearly the same performance as the “k_eq = 20, 4.0 oz” lines. The significance of this will be discussed shortly.

What sort of via designs lead to values of k_{eq} in the range plotted? Starting with size and quantity, Figure 6 shows nine 0.3 mm diameter vias at a 1.0 mm pitch, on a 2.75 mm pad. Figure 7 shows eighteen 0.3 mm diameter vias on a staggered 0.8 mm pitch (a diagonal pitch of 0.57 mm). Equation 2 may be used to calculate the effective conductivity of the two patterns (which, insofar as Equation 2 is concerned, differ only in the total number of vias). If the vias are filled with copper, Equation 2 yields a value of k_{eq} for the Figure 6 configuration of 32 W/m/°C; for that of Figure 7, 64 W/m/°C. On the other hand, if the via diameter were increased to 0.5 mm in the Figure 6 pattern, k_{eq} increases to 89 W/m/°C. (Note that larger vias are probably not feasible for the Figure 7 pattern, as they get too close together and the board falls apart during drilling.)

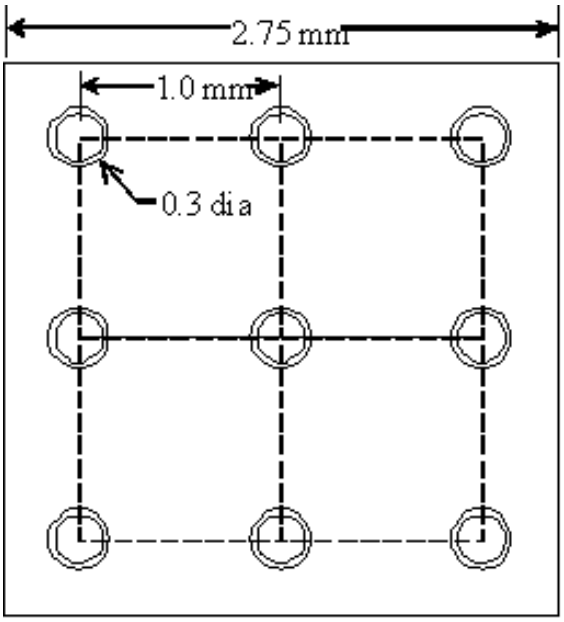

Figure 6. Possible 9−via Pattern for NCS5650

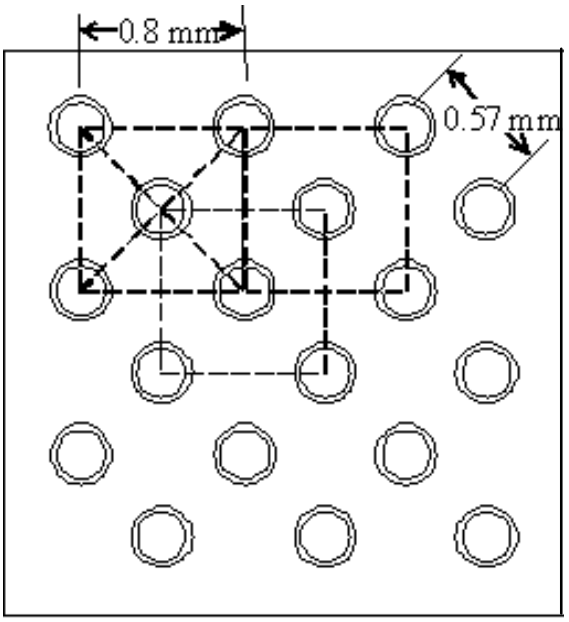

Figure 7. Possible 18−via Pattern for NCS5650

Consider the effect of *not* filling the vias with copper (in which case, the wall thickness becomes very significant). If the vias are unfilled (not recommended, as they will draw solder from the mounting surface during package mounting reflow), for the original Figure 6 pattern and 25 μm via walls, k_{eq} drops all the way to 10.2 W/m/°C. Doubling the wall thickness to 50 μm virtually doubles k_{eq} to 18.3 W/m/°C (as this nearly doubles the cross−section of the wall, hence the amount of copper). In contrast, with the original 25 μm walls, but filling with silver−filled epoxy (k_f =4 W/m/°C), the improvement over unfilled is negligible, with k_{eq} only 10.5 W/m/°C. Even when filled with a 50 W/m/°C solder, k_{eq} rises to only 13 W/m/°C.

Clearly, then, if at all possible, vias should be filled with copper, and as many used as possible in the area available within the mounting pad. This maximizes the heat path from the NCS5650 to the spreader plane. Lest the additional copper in the vias seem to be a negative cost factor, to put the tradeoff between maximal vias and thicker spreader planes in perspective, the amount of additional copper required to fill eighteen 0.3 mm diameter, 25 μm wall vias is only about 0.6 mm^3. The amount of additional copper required to double a 100 mm^2 spreader plane from 2 to 4 oz is 7 mm^3, more than 10x as much. The amount of additional copper required to increase a 100 mm^2, 2 oz spreader, to 400 mm^2, is 28 mm^3. Putting more copper into the vias, whether through number, diameter, wall thickness, or filling, is the right place to put it.

Board Thermal Design

Thermal vias, however, are only part of the story. Significant spreader area must be provided, and aside from raw area, the key to a successful spreader design is that it be “unbroken” insofar as possible. If the plane serves a dual thermal/electrical purpose, for instance being an electrical ground plane, it must be recognized that whereas fairly small webs of copper suffice to keep the plane *electrically* unified, they can seriously undermine the thermal effectiveness. So−called “spider” vias, for instance, should not be used as the thermal connection between the device pad and the spreader plane, as shown in Figure 8.

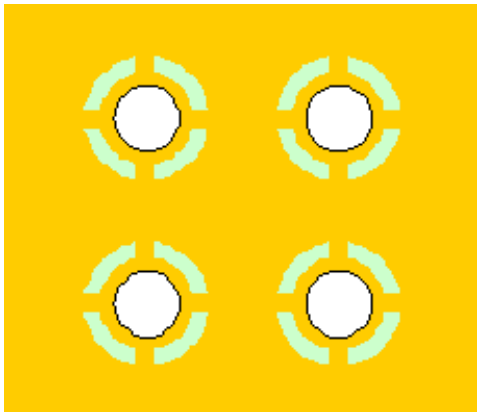

Figure 8. “Spider” Vias

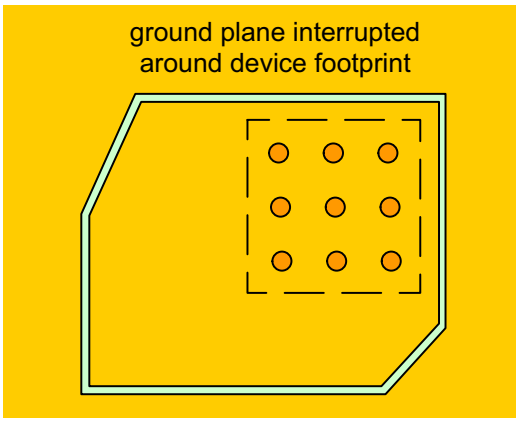

Figure 9. Poor Spreader Design

Similarly, as shown in Figure 9, a small break in the thermal spreader around the package, in order to provide electrical isolation for the pad, can have a serious negative impact on its thermal performance (see Appendix A). However, even though the spreader in Figure 9 is interrupted, the copper area outside the break is not irrelevant – it’s just that if that outer area had been included when estimating θ_{JA}, performance will be significantly worse than expected. Similarly, especially for spreaders that are not much larger than the package footprint, *effective* area is actually somewhat larger than the spreader. The point *here* is that the θ_{JA} values indicated back in Figures 4 and 5 do depend somewhat on more board area than implied in the spreader alone. As the spreader becomes *very* large compared to the package (say 700 mm^2 or larger), the influence of the board beyond the spreader becomes negligible; but for smaller spreaders (again, consider Figure 9), it is a serious error to assume that area beyond the spreader is available for *other* heat sources without impacting the performance of the device in question. The moral is, in complex systems where thermal performance is critical, there is no substitute for a careful system−level thermal analysis taking into account all the geometry, device interactions, and thermal boundary conditions.

Some additional general conclusions can be reached from the models used to generate Figures 4 and 5. Perhaps the most important is that unless a minimum 70 um (2 oz) thick thermal spreader is used, system θ_{JA} cannot be reduced to a value as low as 30°C/W *regardless* of spreader area. A second conclusion is that to achieve values even as low as 40°C/W, *at least* 400 mm^2 of spreader area must be provided, and possibly as much as 700 mm^2, depending, of course, on the k_{eq} value from the via design.

Surface Spreader or Internal Spreader?

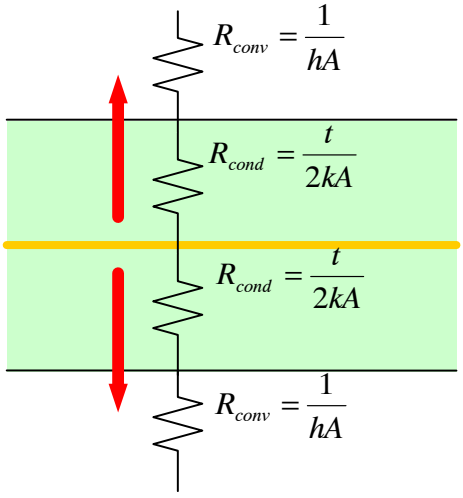

Figure 10. Spreader Plane Centered in Board

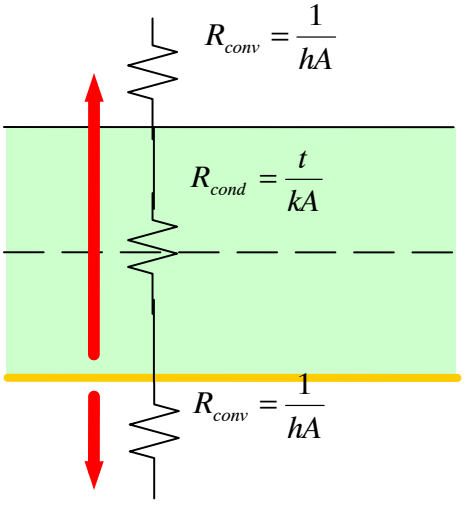

Figure 11. Spreader Plane on Surface of Board

It is often asked whether a thermal spreader must be on the surface of a PCB in order to be effective. In general, the answer is no. This may be seen from a simple analysis of the two extremes shown in Figures 10 and 11. For the sake of this analysis, we assume that the spreader plane is the "source" of heat being dissipated within the board, and we presume that there are equal air flow conditions on the top and bottom surfaces of the board, leading to equal film coefficients, *h*, on each side (Note 2). We also assume that heat flow is purely perpendicular to the plane of the board, meaning that the area associated with these resistance values is the same A in all cases (moreover, it cancels out in the end). With these simplifying assumptions, then if the spreader plane is centered in a board of thickness *t*, the net thermal resistance (equal heat flow up and down, by symmetry), can be shown to be:

$$R_{centered} = \frac{1}{hA}\left(\frac{2k + ht}{4k}\right) \quad \text{(eq. 3)}$$

For the surface spreader, the net thermal resistance can be shown to be:

$$R_{surface} = \frac{1}{hA}\left(\frac{k + ht}{4k}\right) \quad \text{(eq. 4)}$$

It may not be evident at this point, but it will be seen that the centered spreader always has a higher resistance than the surface spreader. In anticipation of the result, we therefore compute the fractional excess of the centered spreader thermal resistance over the surface spreader value as follows:

$$\frac{R_{centered}}{R_{surface}} - 1 = \frac{\left(\frac{2k+ht}{4k}\right)}{\left(\frac{k+ht}{2k+ht}\right)} - 1 = \frac{(2 + Bi)^2}{4(1 + Bi)} - 1 = \frac{Bi^2}{4(1 + Bi)} \quad \text{(eq. 5)}$$

where Bi = ht/k, the Biot number.

The result is clearly positive−definite. Consider, then, typical values for the significant parameters: A still−air film coefficient will be on the order of 20 W/m^2/°C. Board out−of−plane conductivity will be on the order of 0.3 W/m/°C. A typical board will have a thickness of 0.0015 m. Therefore a typical Biot number will be roughly 0.1, and the fractional increase of the centered−spreader resistance over the comparable surface−spreader resistance will be only 0.0022 (= 0.01/4/1.1), or 0.2%. Plainly, it doesn't make much difference to the overall cooling capability of the spreader, as to whether it's buried within the PCB, or at the surface. Making the board of a more conductive material, or thinner, will mitigate the effect even more. Conversely, increasing the film coefficient by improving the air flow (or changing the cooling fluid from air to a liquid), will increase the penalty of burying the spreader. All else being equal, even if the film coefficient increases by a factor of five, to 100 W/m^2/°C, the fractional cost of burying the spreader is still only 4%; if it increases tenfold, to 200 W/m^2/°C, we begin to see a significant degradation (if 12.5% seems significant) (Note 3).

Summary

Undeniably, certain gross package parameters (such as footprint) will have an influence on the overall thermal performance of a system. In most cases, however, the package is the least significant factor in achieving overall thermal design success. The variables that matter most, independent of the package choice, are in the details of thermal "communication" between the device and the external ambient. The number−one variable is the available heat spreading surface, controlled first by its uninterrupted area, and second by its thickness. This is followed closely by the thoughtful use and details in the design of thermal vias. Even when these factors are taken into account, external boundary conditions (air flow rate, neighboring heat sources, and board area beyond the designated heat spreader for the device in question) must be considered. The NCS5650 provides excellent thermal performance when the system surrounding it has been subjected to a thorough thermal analysis and designed with high performance in mind.

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2. As a rule, convection from the surface of a board depends on the airflow conditions, not the surface material properties. Thermal radiation is an exception: shiny surfaces tend to radiate more poorly than dull, diffuse surfaces; thus an exposed metal spreader may actually lose *less* heat than bare PCB material. Worse, in still air environments, radiation may account for 30% or more of the heat transfer.
3. For purposes of illustration, textbook flat plate heat transfer coefficients of 100 W/m^2/°C may require air velocities on the order of 8 m/s, which is substantial; 200 W/m^2/°C requires more like 30 m/s (Mach 0.1).

APPENDIX A – EFFECT OF BREAKS OR GAPS IN THERMAL SPREADERS

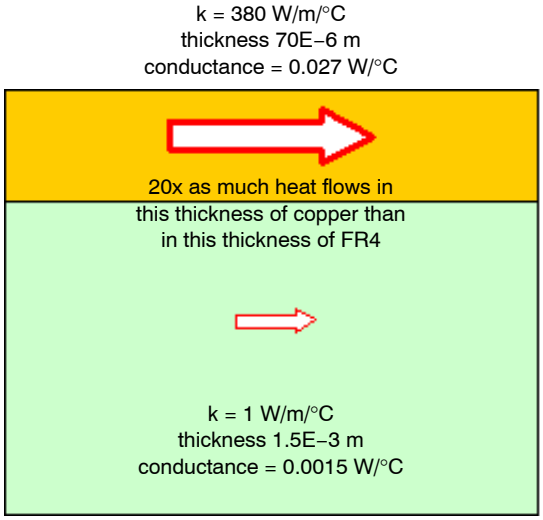

Figure 12. A Continuous Spreader Plane

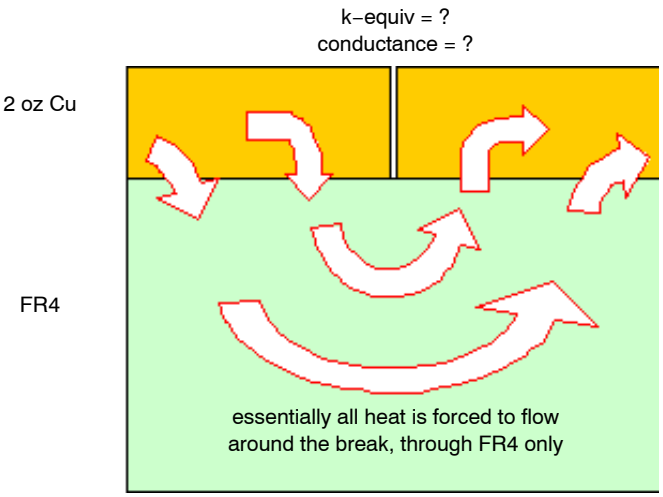

Figure 13. A Discontinuous Spreader Plane

To see the effect of a small break in a spreader plane (such as depicted in Figure 9 in the main body of this report), consider the difference between the heat flow shown in Figures 12 and 13.

Qualitatively, we see that when the spreader is continuous, the FR4 contributes very little to the overall thermal picture. The “conductance” values shown (the product of conductivity and cross−sectional path width) are actually per unit width (i.e. depth into the page) and per unit length of the flow path, so they don’t translate directly into thermal resistances without specifying additional parameters. Even so, the analysis is simple in principle, so long as the spreader and board area in question are far from a heat source, and heat flow is thus primarily horizontal (in the plane of the board). Unfortunately, the equivalent conductance in the “discontinuous” case does not lend itself to simple closed−form analysis, due to the finite thicknesses involved, the fact that a small amount of heat can actually “leap” the gap (depending on gap details), and the fact that FR4 tends to have orthotropic thermal conductivity (different in−plane than through−plane values).

Figure 14 presents the results obtained from a 2D finite element model exploring the increase in board resistance (per unit depth into the page) of a discontinuous spreader plane.

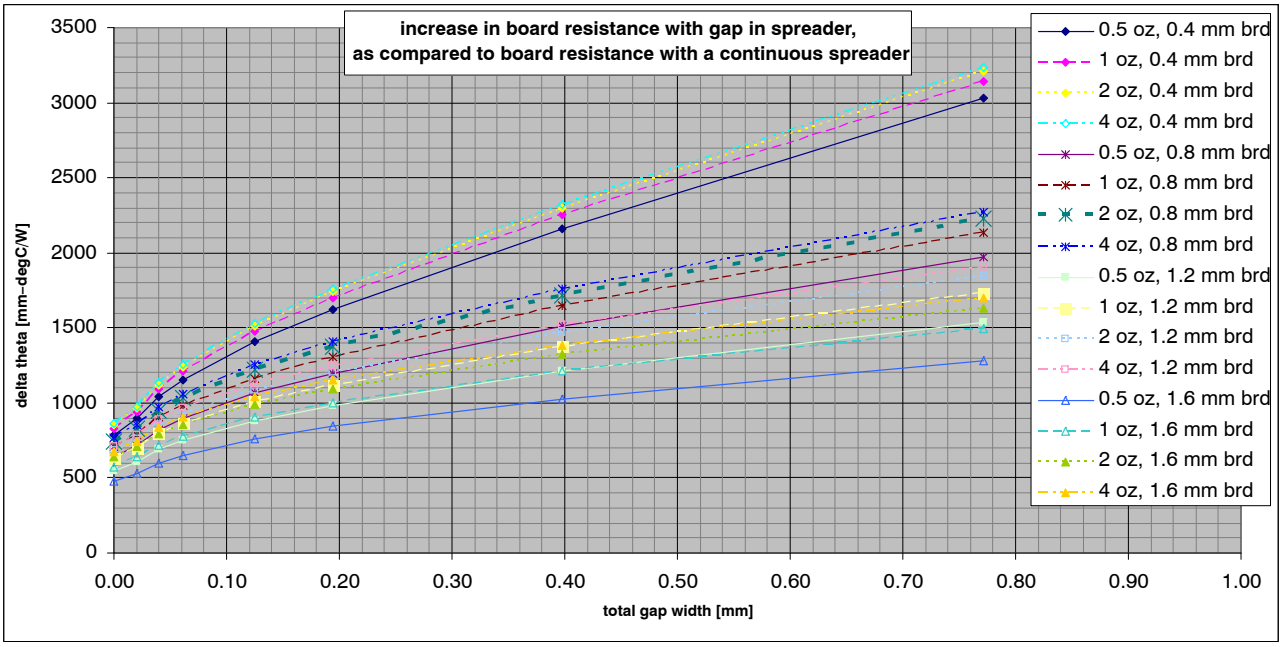

Figure 14. Increase in Board Thermal Resistance Due to Discontinuous Heat Spreader

In this model, parameters of significant interest are the ratio of spreader thickness to board thickness, and the actual width of the gap (from zero to several times the spreader thickness). Boundary conditions are imposed at a distance of several board thicknesses to the left and right of the break, and the difference in thermal resistance (per unit depth into the page) was computed between the discontinuous model and the continuous model. The first thing to notice is that the increase in resistance does not go to zero as the gap width goes to zero. This is expected from the qualitative analysis of Figures 12 and 13. In the specific case of 70 um thick Cu (2 oz) on a 0.8 mm FR4 board, it is seen that the minimum increase in resistance is roughly 750 mm−°C/W. Thus, if one had a continuous spreader covering the back side of a circuit board, and then inscribed a circular cut in this spreader at a 10 mm radius around a heat source (say a 4x4 QFN), the circumference of this cut would be 62 mm, and the immediate increase in thermal resistance of the board simply due to the presence of the cut would be roughly 12°C/W (i.e., 750/62). If the spreader area had been sized for, say, 30°C/W, this would imply a 40% increase in thermal resistance! Further, if the “cut” was actually a designed−in gap, then depending on board layout design rules, it would surely have a finite width of more like 0.2 mm minimum.

Whereas this clearly emphasizes that breaks in spreader planes are serious and must be avoided, on the other hand, it may not be *quite* as bad as this initial analysis suggests. After all, the farther from the heat source the break, the more heat has already been dissipated (by convection) from the spreader area prior to reaching the break. A more careful analysis yields plots as shown in Figures 15, 16, and 17, where an axisymmetric board model of a square 50 mm spreader on a 0.8 mm thick FR4 board has been simulated. In Figure 15, the spreader is unbroken; in Figures 16 and 17, a gap has been inserted into the model at 3/4 the distance out from the center (in Figure 16, the gap is present and breaks the spreader, but has zero width; in Figure 17, the gap has a width of 0.2 mm). The plots show the temperature profile of various thickness spreaders, under otherwise identical boundary conditions.

This analysis shows that whereas the unbroken spreaders yield a board resistance of about 23°C/W (for a 2 mm radius heat source), the spreaders with 0 μm gaps add only a net 2°C/W to the unbroken spreader values, and spreaders with 0.2 mm gaps add perhaps another 1.5°C/W. These amount to somewhat less than 20% of the original value, not the 40% worst−case originally deduced from an analysis that did not take into account heat loss prior to reaching the break in the spreader. Obviously there are many parameters that affect the precise results, but the moral should be clear: continuous planes of copper should be the goal, as heat flow is seriously obstructed by even the smallest discontinuity in the plane.

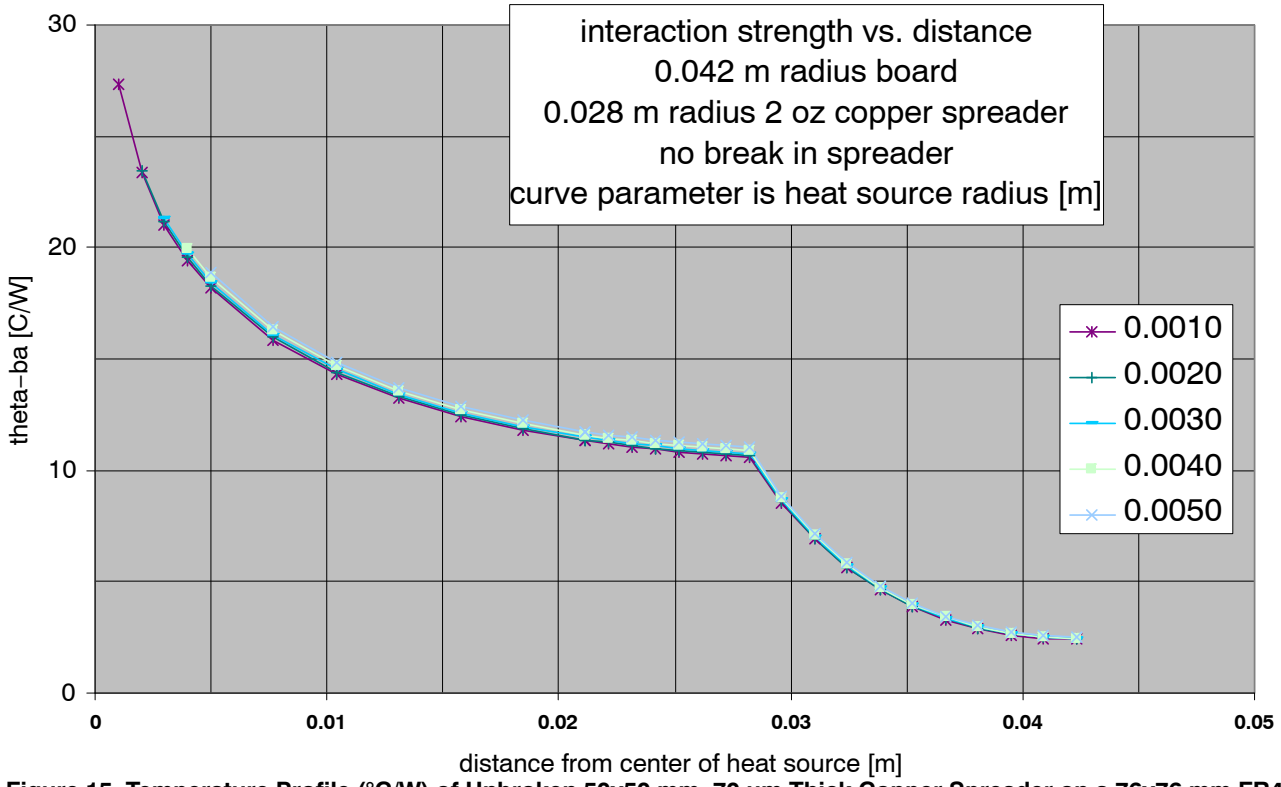

Figure 15. Temperature Profile (°C/W) of Unbroken 50x50 mm, 70 um Thick Copper Spreader on a 76x76 mm FR4 Board

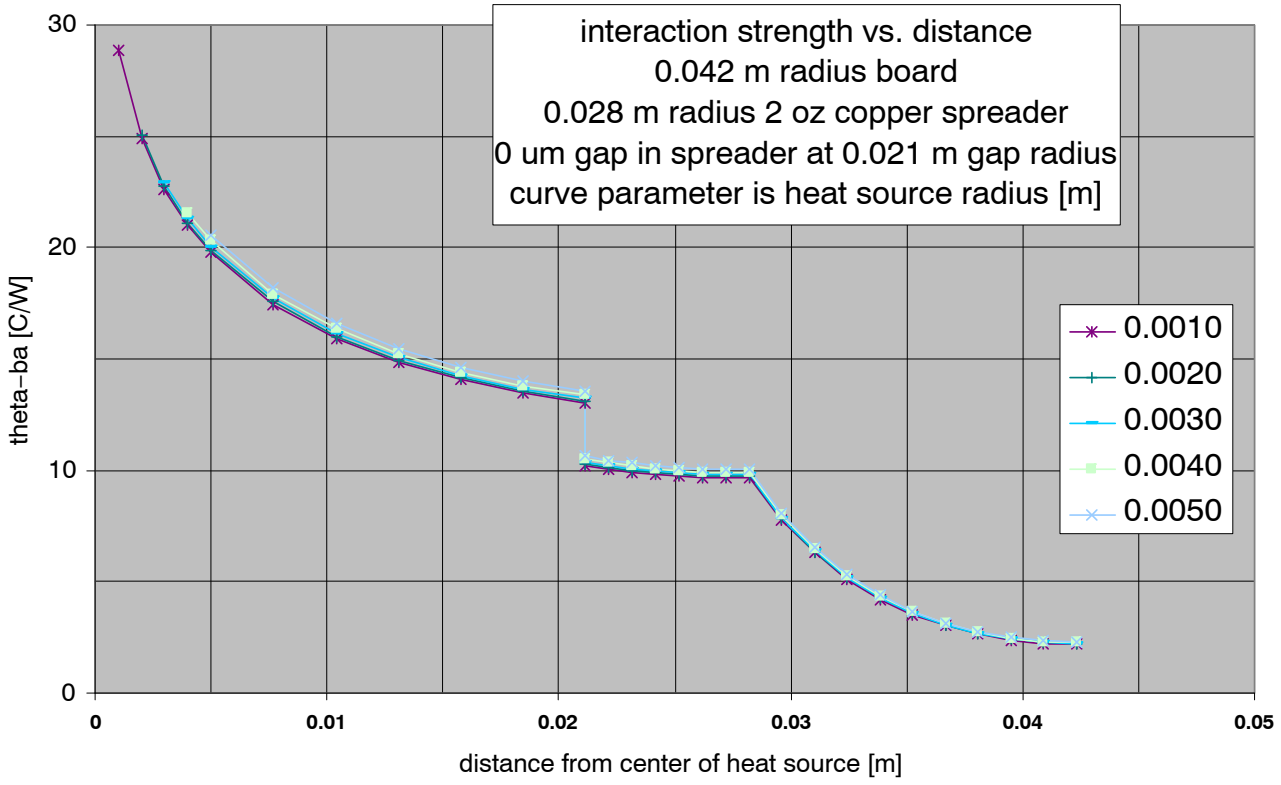

Figure 16. Temperature Profile (°C/W) of 50x50 mm, 70 um Thick Copper Spreader on a 76x76 mm FR4 Board; Spreader has 0 um Discontinuity at a 21 mm Radius from the Heat Source

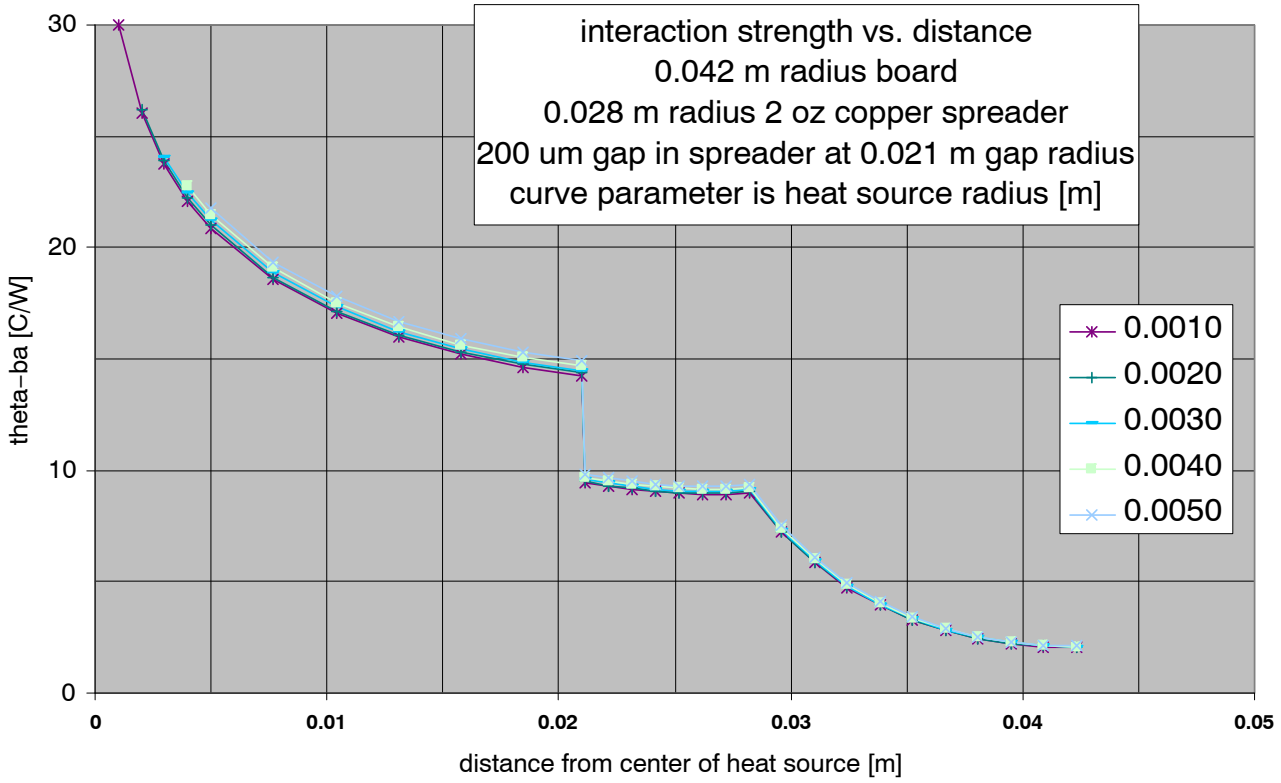

Figure 17. Temperature Profile (°C/W) of 50x50 mm, 70 um Thick Copper Spreader on a 76x76 mm FR4 Board; Spreader has 200 um Discontinuity at a 21 mm Radius from the Heat Source

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